

Amendments to the Specification

Please *replace* the “Related Applications” section of page 1, lines 10-19, with the following:

The present patent application is related to U.S. Patent No. 6,678,796, filed October 3, 2000 and entitled “System and Method for Scheduling Memory Instructions to Provide Adequate Prefetch Latency,” U.S. Patent No. 6,574,713, filed October 10, 2000 and entitled “Heuristic for Identifying Loads Guaranteed to Hit in Processor Cache” and U.S. Patent No. 6,651,245, filed October 3, 2000 and entitled “System and Method for Insertion of Prefetch Instructions by a Compiler.” These patents have been assigned to the same assignee and are incorporated herein by reference.